

IN THE CLAIMS:

1. (Currently Amended) A hybrid substrate comprising:
a carrier substrate having a plurality of pockets patterned thereon; and
at least two substrates, each substrate being formed from a different single-crystal
~~conductive materials~~ and being deposited within a separate ~~each-pocket~~ of the plurality of
pockets, for fabricating a plurality of devices.
2. (Currently Amended) The hybrid substrate according to Claim 1, wherein the at
least two ~~different single-crystal conductive materials~~ substrates are different from each other
and are approximately co-planar with a top surface of the carrier substrate.
3. (Currently Amended) The hybrid substrate according to Claim 1, wherein the at
least two ~~different~~ substrates are different from each other and single-crystal conductive
~~materials~~ are bonded to the carrier substrate.
4. (Currently Amended) The hybrid substrate according to Claim 1, wherein each of
the at least two different substrates ~~single-crystal conductive materials is~~ are selected from the
group consisting of GaAs, InP, silicon (Si), substrate materials for optoelectronic devices, and
GaN-based substrate materials for high-electron mobility transistors (HEMTs).
5. (Currently Amended) The hybrid substrate according to Claim 1, wherein the
carrier substrate is selected from the group consisting of AlN, quartz, glass, ceramic, CVD
diamond, and sapphire.
6. (Currently Amended) The hybrid substrate according to Claim 1, wherein the
carrier substrate is a high thermal conductive substrate.
7. (Cancelled)

8. (Withdrawn) A method for fabricating a hybrid substrate comprising the steps of:

patterning a substrate with a plurality of pockets; and
providing a material within each of the plurality of pockets, wherein at least two materials provided within two respective pockets of the plurality of pockets are different.

9. (Withdrawn) The method according to Claim 8, further comprising the step of planarizing the materials provided within each of the plurality of pockets, such that a top surface of the materials is approximately co-planar with a top surface of the substrate.

10. (Withdrawn) The method according to Claim 9, wherein the planarizing step includes a chem-mech polishing step.

11. (Withdrawn) The method according to Claim 8, further comprising the step of providing a thermal conductivity layer between the substrate and the material provided within each of the plurality of pockets.

12. (Withdrawn) The method according to Claim 10, wherein the thermal conductivity layer is a CVD diamond layer.

13. (Withdrawn) The method according to Claim 8, further comprising the step of providing a layer of oxide over the material provided within each of the plurality of pockets.

14. (Withdrawn) The method according to Claim 13, wherein the layer of oxide is a layer of CVD oxide.

15. (Withdrawn) The method according to Claim 8, further comprising the step of providing an oxide on at least one surface of each material before the step of providing the material within each of the plurality of pockets.

16. (Withdrawn) The method according to Claim 8, further comprising the step of annealing to adhere the material provided within each of the plurality of pockets to the substrate.

17. (Withdrawn) The method according to Claim 8, further comprising the step of preparing the material provided within each of the plurality of pockets with the blister separation method.

18. (Withdrawn) The method according to Claim 8, further comprising the step of applying interconnect structures between the materials provided within the plurality of pockets.

19. (Currently Amended) The hybrid substrate according to Claim 1, wherein each pocket of the plurality of pockets has a greater surface area than a surface area of a cross-section of a substrate ~~the at least two different single crystal conductive materials deposited within that~~ pocket.

20. (New) The hybrid substrate according to Claim 1, wherein the at least two substrates and the carrier substrate are each formed from a different material.